CLAIMS

What is claimed is:

1. A method for determining a logic state of a magnetic tunnel junction (MTJ) memory device, the method comprising:

applying a first bias voltage to a selected line;

measuring a first induced voltage across the MJT device;

applying a second bias voltage to the selected line, the second bias voltage being different from the first bias voltage;

measuring a second induced voltage across the MJT device; and

comparing a function of two or more of the first bias voltage, the first induced voltage, the second bias voltage, and the second induced voltage to a threshold value.

2. The method of claim 1, wherein the second bias voltage is less than the first bias voltage.

3. The method of claim 1, wherein the second bias voltage is greater than the first bias voltage.

4. The method of claim 1, wherein comparing the function of the two or more of the first bias voltage, the first induced voltage, the second bias voltage, and the second induced voltage to the threshold value comprises comparing a ratio of a first ratio of the second induced voltage to the second bias voltage and a second ratio of the first induced voltage to the first bias voltage to the threshold.

5. The method of claim 4, wherein the threshold is one.

6. The method of claim 4, wherein the threshold is a ratio of the tunneling magneto resistance ratio (TMR) at the first bias voltage and the second bias voltage.

7. The method of claim 1, wherein measuring the first induced voltage across the MJT device comprises measuring the voltage across a sneak resistance of the MJT device; and wherein measuring the second induced voltage across the MJT device comprises measuring the voltage across the sneak resistance of the MJT device.

8. The method of claim 1, wherein the MTJ device is a magnetic random access memory (MRAM).

9. The method of claim 8, wherein the MRAM is an MRAM array.

10. The method of claim 1, wherein applying the first bias voltage to a selected line comprises applying a first row voltage to the selected line while applying a first lesser voltage than the first row voltage to non-selected lines; and wherein applying the second bias voltage to the selected line, the second bias voltage being different from the first bias voltage comprises applying a second row voltage to the selected line while applying a second lesser voltage than the second row voltage to non-selected lines.

11. The method of claim 10, wherein applying the first row voltage to the selected line while applying the first lesser voltage than the first row voltage to non-selected lines comprises applying the first row voltage to the selected line while grounding the non-selected lines; and wherein applying the second row voltage to the selected line while applying a second lesser voltage than the second row voltage to non-selected lines comprises applying the second row voltage to the selected line while grounding the non-selected lines.

12. A system for determining the logic state of a magnetic tunnel junction (MTJ) memory device, the system comprising:

a biasing circuit configured to supply at least two different biasing voltages to a selected line;

a sensing circuit configured to measure the across the MTJ device at each of the at least two different biasing voltages; and

a processing element configured to compare a function of at least two of the first bias voltage, the first induced voltage, the second bias voltage, and the second induced voltage to a threshold value.

13. The system of claim 12, wherein the biasing circuit, the sensing circuit, the processing element and the MTJ device are fabricated as an application specific integrated circuit (ASIC).

14. The system of claim 12, wherein the biasing circuit is a voltage supply.

15. The system of claim 12, wherein the sensing circuit is a voltmeter.

16. The system of claim 12, wherein the MTJ device is a magnetic random access memory (MRAM).

17. The system of claim 16, wherein the MRAM is an MRAM array.

18. A memory comprising an array of MTJ cells configured to accept a bias voltage for a selected memory cell along a first line and to provide a read voltage across the sneak resistance of the array of MTJ cells to a read logic along a second line.

19. The memory of claim 18, further comprising:

a memory controller configured to receive one or more inputs;

a biasing circuit configured to provide the bias voltage to the selected memory cell at least twice with different voltage values; and

the read logic configured to receive the read voltage across the sneak resistance of the array of MTJ cells for each of the difference voltage values.

20. The memory of claim 19, further comprising:

decision logic configured to receive at least the read voltage across the sneak resistance of the array of MTJ cells for each of the difference voltage values, wherein the decision logic is further configured to determine a function value using at least the read voltage across the sneak resistance of the array of MTJ cells for each of the difference voltage values and to compare the function value to a threshold value.

21. The memory of claim 20, further comprising:

one or more storage locations.

22. The memory of claim 21, wherein the one or more storage locations are assessable to the decision logic and the read logic and configured to store one or more of a first bias voltage, a first induced voltage, a second bias voltage, a second induced voltage, and the threshold value.

23. A system, comprising:

a processor;

a memory assessable to the processor, wherein the memory includes a memory comprising an array of MTJ cells configured to accept a bias voltage for a selected memory cell along a first line and to provide a read voltage across the sneak resistance of the array of MTJ cells to a read logic along a second line.

24. The system of claim 23, the memory further comprising:
a memory controller configured to receive one or more inputs;
a biasing circuit configured to provide the bias voltage to the selected memory cell at least twice with different voltage values; and
the read logic configured to receive the read voltage across the sneak resistance of the array of MTJ cells for each of the difference voltage values.

25. The system of claim 24, the memory further comprising:
decision logic configured to receive at least the read voltage across the sneak resistance of the array of MTJ cells for each of the difference voltage values, wherein the decision logic is further configured to determine a function value using at least the read voltage across the sneak resistance of the array of MTJ cells for each of the difference voltage values and to compare the function value to a threshold value.

26. The system of claim 25, the memory further comprising:
one or more storage locations.

27. The system of claim 26, wherein the one or more storage locations are assessable to the decision logic and the read logic and configured to store one or more of a first bias voltage, a first induced voltage, a second bias voltage, a second induced voltage, and the threshold value.

28. A memory, comprising:
an array of MTJ cells configured to accept a bias voltage for a selected memory cell along a first line and to provide a read voltage across the selected memory cell to a read logic along a second line;
a memory controller configured to receive one or more inputs;

a biasing circuit configured to provide the bias voltage to the selected memory cell at least twice with different voltage values; and

the read logic configured to receive the read voltage across the selected memory cell for each of the difference voltage values.

29. The memory of claim 28, further comprising:

decision logic configured to receive at least the read voltage across the selected memory cell for each of the difference voltage values, wherein the decision logic is further configured to determine a function value using at least the read voltage across the selected memory cell for each of the difference voltage values and to compare the function value to a threshold value.